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EXAMINER
CHANG, EDITH M

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 04/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,776	MEDLOCK, JOEL D.	
	Examiner	Art Unit	
	Edith M Chang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-33 and 35-41* is/are rejected.

7)☒ Claim(s) *14 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the second page of drawings should be "PRIOR ART FIGURE 1C" in stead of "PRIOR ART FIGURE 1B" which shown in the first page of the drawings.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Fill the application serial number in line 34, Page 12, and line 16, page 13.

Page 19, line 16, "Galois field 254" wherein the 254 is in the Fibonacci field.

Page 19, lines 33-34, the "input 430" is not found in Figure 4.

Appropriate corrections are required.

Claim Objections

3. Claims 1-14, 24, 34, and 40-41 are objected to because of the following informalities:

Claim 1, line 5, spell out the LFSR when it is recited in the claim.

Claim 9, line 13, spell out the LFSR when it is recited in the claim.

Claim 13, add legend of N, its characteristics and range, when it is recited in the claim.

Claim 24, add legend of N, its characteristics and range, when it is recited in the claim.

Claim 34, add legend of N, its characteristics and range, when it is recited in the claim.

Claims 40, "The code generator system recited in Claim 35 further comprising the step of:" wherein the claim 35 is an apparatus claim of a code generator system comprising elements which the apparatus is composite of, not step.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-13, and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Brown et al. (US 6282230 B1).

Regarding **claims 1-3**, Brown et al. discloses the method of calculating a mask for a desired code offset in an LFSR comprising the steps of: *a)* receiving the desired code offset from a reference code state chosen for a first field (column 7 lines 3-10, column 7 line 60-column 8 line 5, the circuitry performing the matrix calculation shown in U.S. Ser. No. 09/222,454 is now U.S. Patent 6173009 where FIG.2/FIG.5/column 5 lines 1-45 '009 is the first field in Galois form, FIG.5 the offset j is the desired code offset, current position is the reference code state chosen); *b)* calculating a first field vector in the first field with the desired code offset sought in

the first field (column 5 lines 1-45 equation [12] '009); and *c)* transforming the first field vector into a second field vector in a second field/Fibonacci form, the second field vector operable as a mask in the LFSR configured in the first field (40 Fig.5, column 6 lines 29-35, column 7 lines 3-10 wherein using the Galois LFSR to get the Fibonacci mask, 56 FIG.5) by multiplying the Galois field vector by a transformation matrix to obtain the Fibonacci field vector (column 7 lines 5-8, s[n] is the Galois field, FIG.5 S[] is the Fibonacci field vector).

Regarding **claim 4**, Brown et al. discloses the transformation matrix is a linear NxN matrix, and wherein N is the degree of the polynomial that defines the Fibonacci field and Galois field (column 3 line 30-column 4 line 35, column 5 line 55-column 6 line 30, where the T/F is a linear 4x4 matrix, 4 is the degree of the polynomial '230; column 5 lines 35-45 '009).

Regarding **claims 5 & 6**, Brown et al. discloses the reference code state in the Galois field corresponds to the reference code state in the Fibonacci field (FIG.5 when the code state is in Fibonacci form, in 40 is Galois form), further comprising the step of d) transforming the reference code state from the Fibonacci field to the reference code state in the Galois field (FIG.5 40 where the reference code state is transformed from the Fibonacci field to Galois field, column 3 lines 30-65 & column 5 lines 35-65, column 6 lines 20-25).

Regarding **claim 7**, Brown et al. discloses the step of e) calculating the Galois field vector corresponding to the desired code offset from the reference code state in the Galois field (column 3 lines 30-column 4 lines 35, where the offset can be calculated using repeated application).

Regarding **claim 8**, Brown et al. discloses the step of multiplying the field vector representing the reference code state in the Fibonacci field by a transformation matrix to obtain a

subsequent field vector representing the reference code state vector in the Galois field (FIG.5 the current position n in PN sequence is in the Fibonacci field, via 40 which multiplies a transformation matrix to obtain a subsequent field vector representing the reference code state vector in the Galois field wherein the 40 is the Galois LFSR).

Regarding **claims 9 & 10**, Brown et al. discloses the method of calculating a transform matrix for transforming a field vector from a second field to a field vector in a first field, the method comprising the steps of: a) receiving a reference code state chosen for the first field (column 7 lines 3-10, the circuitry performing the matrix calculation shown in U.S. Ser. No. 09/222,454 is now U.S. Patent 6173009 where FIG.2/FIG.5/column 5 lines 1-45 '009 is the first field in Galois form, FIG.5 the offset j is the desired code offset, current position is the reference code state chosen); b) generating a first field vector of the reference code state (column 5 lines 1-45 equation [12] '009; c) iterating an LFSR state from the first field vector to form a new LFSR state (column 3 lines 30-column 4 lines 35, where the offset can be calculated using repeated application, and form a new LFSR state, column 5 line 30-column 6 line 30 the n+1 new state); d) generating a new field vector from the new LFSR state (column 5 line 30-column 6 line 30, the s[n+1] is the new field vector); and e) assembling the first field vector and the new field vector into a transform matrix (40 FIG.5, column 5 line 30-column 6 line 30, the F is the transform matrix).

Regarding **claims 11 & 12**, Brown et al. discloses the step of identifying an output tap location of an LFSR in the first field from which an output sequence is received and aligning the reference code state in the first field vector with the output tap location of the LFSR (40 FIG.5/42 FIG.4 implemented by Galois LFSR FIG.5 '009).

Regarding **claim 13**, Brown et al. discloses repeating steps c) through d) of claim 9 N times, wherein N is the degree of the polynomial defining the first filed and the second field (column 3 lines 30-column 4 lines 35, where N is 4 in the design chosen polynomial, column 5 lines 35-45 [13] '009).

Regarding **claim 15**, Brown et al. discloses a method of advancing a state of a Galois LFSR by a code offset (FIG.5), the method comprising the steps of: a) receiving a Fibonacci mask corresponding to the code offset for the Galois LFSR (FIG.5, input 40, the current position N in PN sequence is the mask corresponding to); b) loading the Fibonacci mask in the Galois LFSR (40 FIG.5, column 7 lines 3-10, column 7 line 60-column 8 line 5, the circuitry performing the matrix calculation shown in U.S. Ser. No. 09/222,454 is now U.S. Patent 6173009 where FIG.2/FIG.5/column 5 lines 1-45 '009 is the first field in Galois form); c) iterating the Galois LFSR according to the Fibonacci mask (column 3 lines 30-column 4 lines 35, where the offset can be calculated using repeated application, and form a new LFSR state, column 5 line 30-column 6 line 30 the n+1 new state); and d) receiving an output from the Galois LFSR corresponding to the code offset (FIG.5 output 40).

Regarding **claims 16 & 17**, Brown et al. discloses e) identifying a desired code offset for the Galois LFSR (40 FIG.5); f) selecting the Fibonacci mask that exactly matches the desired code offset (56 FIG.5); and g) slewing the Galois LFSR to attain the desired code offset (FIG.5, column 5 lines 35-65, wherein the Galois LFSR slewing/speding to attain the desired code offset '009)

Regarding **claim 18**, Brown et al. discloses storing the Fibonacci mask in memory (56 FIG.5).

Regarding **claim 19**, Brown et al. discloses e) receiving a request to advance the Galois LFSR by the code offset (FIG.5 input of 40).

Regarding **claim 20**, Brown et al. discloses e) calculating the Fibonacci mask corresponding to the desired code offset (56 FIG.5).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 21-33, and 35-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (US 6282230 B1) in view of Asano (US 6295301).

Regarding **claims 21-23**, except explicitly specify the program instructions executed by the processor for the method, Brown et al. discloses the method of comprising the steps of: *a)* receiving the desired code offset from a reference code state chosen for a first field (column 7 lines 3-10, column 7 line 60-column 8 line 5, the circuitry performing the matrix calculation shown in U.S. Ser. No. 09/222,454 is now U.S. Patent 6173009 where FIG.2/FIG.5/column 5 lines 1-45 '009 is the first field in Galois form, FIG.5 the offset j is the desired code offset, current position is the reference code state chosen); *b)* calculating a first field vector in the first field with the desired code offset sought in the first field (column 5 lines 1-45 equation [12] '009); and *c)* transforming the first field vector into a second field vector in a second field/Fibonacci form, the second field vector operable as a mask in the LFSR configured in the

first field (40 Fig.5, column 6 lines 29-35, column 7 lines 3-10 wherein using the Galois LFSR to get the Fibonacci mask, 56 FIG.5) by multiplying the Galois field vector by a transformation matrix to obtain the Fibonacci field vector (column 7 lines 5-8, s[n] is the Galois field), however Asano discloses the processor and the computer program for the PN code generator (column 8 line 65-column 9 line 5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the processor and program/software taught by Asano implementing the Brown et al.'s PN code generator to have a efficient code generator to reduce the power consumption (column 9 lines 5-20).

Regarding **claim 24**, Brown et al. discloses the transformation matrix is a linear NxN matrix, and wherein N is the degree of the polynomial that defines the Fibonacci field and Galois field (column 5 lines 55-65, where the F is a linear 4x4 matrix, 4 is the degree of the polynomial).

Regarding **claims 25 & 26**, Brown et al. discloses the reference code state in the Galois field corresponds to the reference code state in the Fibonacci field (FIG.5 when the code state is in Fibonacci form, in 40 is Galois form), further comprising the step of d) transforming the reference code state from the Fibonacci field to the reference code state in the Galois field (FIG.5 40 where the reference code state is transformed from the Fibonacci field to Galois field, column 3 lines 30-65 & column 5 lines 35-65, column 6 lines 20-25).

Regarding **claim 27**, Brown et al. discloses the step of e) calculating the Galois field vector corresponding to the desired code offset from the reference code state in the Galois field (column 3 lines 30-column 4 lines 35, where the offset can be calculated using repeated application).

Regarding **claim 28**, Brown et al. discloses the step of multiplying the field vector representing the reference code state in the Fibonacci field by a transformation matrix to obtain a subsequent field vector representing the reference code state vector in the Galois field (FIG.5 the current position n in PN sequence is in the Fibonacci field, via 40 which multiplies a transformation matrix to obtain a subsequent field vector representing the reference code state vector in the Galois field wherein the 40 is the Galois LFSR).

Regarding **claims 29 & 30**, except explicitly specify the program instructions executed by the processor for the method, Brown et al. discloses the method of calculating a transform matrix for transforming a field vector from a second field to a field vector in a first field, the method comprising the steps of: a) receiving a reference code state chosen for the first field (column 7 lines 3-10, the circuitry performing the matrix calculation shown in U.S. Ser. No. 09/222,454 is now U.S. Patent 6173009 where FIG.2/FIG.5/column 5 lines 1-45 '009 is the first field in Galois form, FIG.5 the offset j is the desired code offset, current position is the reference code state chosen); b) generating a first field vector of the reference code state (column 5 lines 1-45 equation [12] '009; c) iterating an LFSR state from the first field vector to form a new LFSR state (column 3 lines 30-column 4 lines 35, where the offset can be calculated using repeated application, and form a new LFSR state, column 5 line 30-column 6 line 30 the n+1 new state); d) generating a new field vector from the new LFSR state (column 5 line 30-column 6 line 30, the s[n+1] is the new field vector); and e) assembling the first field vector and the new field vector into a transform matrix (column 5 line 30-column 6 line 30, the F is the transform matrix), however Asano discloses the processor and the computer program for the PN code generator (column 8 line 65-column 9 line 5). At the time of the invention, it would have been

obvious to a person of ordinary skill in the art to have the processor and program/software taught by Asano implementing the Brown et al.'s PN code generator to have a efficient code generator to reduce the power consumption (column 9 lines 5-20).

Regarding **claims 31 & 32**, Brown et al. discloses the step of identifying an output tap location of an LFSR in the first field from which an output sequence is received and aligning the reference code state in the first field vector with the output tap location of the LFSR (40 FIG.5/42 FIG.4 implemented by Galois LFSR FIG.5 '009).

Regarding **claim 33**, Brown et al. discloses repeating steps c) through d) of claim 9 N times, wherein N is the degree of the polynomial defining the first filed and the second field (column 3 lines 30-column 4 lines 35, where N is 4 in the design chosen polynomial, column 5 lines 35-45 [13] '009).

Regarding **claim 35**, except explicitly specify the program instructions executed by the processor for/coupled the LFSR, Brown et al. discloses a method of advancing a state of a Galois LFSR by a code offset (FIG.5), the method comprising the steps of: a) receiving a Fibonacci mask corresponding to the code offset for the Galois LFSR (FIG.5, input 40, the current position N in PN sequence is corresponding the mask); b) loading the Fibonacci mask in the Galois LFSR (40 FIG.5, column 7 lines 3-10, column 7 line 60-column 8 line 5, the circuitry performing the matrix calculation shown in U.S. Ser. No. 09/222,454 is now U.S. Patent 6173009 where FIG.2/FIG.5/column 5 lines 1-45 '009 is the first field in Galois form); c) iterating the Galois LFSR according to the Fibonacci mask (column 3 lines 30-column 4 lines 35, where the offset can be calculated using repeated application, and form a new LFSR state, column 5 line 30-column 6 line 30 the n+1 new state); and d) receiving an output from the Galois

LFSR corresponding to the code offset (FIG.5 output 40). However Asano discloses the processor and the computer program for the PN code generator (column 8 line 65-column 9 line 5), at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the processor and program/software taught by Asano implementing the Brown et al.'s PN code generator to have a efficient code generator to reduce the power consumption (column 9 lines 5-20).

Regarding **claims 36 & 37**, Brown et al. discloses e) identifying a desired code offset for the Galois LFSR (40 FIG.5); f) selecting the Fibonacci mask that exactly matches the desired code offset (56 FIG.5); and g) slewing the Galois LFSR to attain the desired code offset (FIG.5, column 5 lines 35-65, wherein the Galois LFSR slewing/speding to attain the desired code offset '009)

Regarding **claim 38**, Brown et al. discloses storing the Fibonacci mask in memory (56 FIG.5).

Regarding **claim 39**, Brown et al. discloses e) receiving a request to advance the Galois LFSR by the code offset (FIG.5 input of 40).

Regarding **claim 40**, Brown et al. discloses calculating a transform matrix corresponding to a Fibonacci LFSR equivalent to the Galois LFSR (column 7 lines 3-10, column 7 line 60-column 8 line 5, where the F is the transform matrix corresponding to a Fibonacci LFSR equivalent to the Galois LFSR).

Regarding **claim 41**, Brown et al. discloses calculating the mask corresponding to the desired code offset using the transform matrix (FIG.5 40 to 58).

Allowable Subject Matter

8. Claims 14 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcome the objections stated in paragraph 2.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
March 25, 2004

CHIEH M. FAN
PRIMARY EXAMINER